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EXAMINER	
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ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,093	WURZBURG, HENRY	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-44 have been presented for examination in this application. In response to the last Office Action, none of the claims were canceled. As the result, claims 1-44 are now pending in this application.

Claims 1-44 are rejected.

Applicant's arguments filed 7/5/06 have been fully considered, with the results that follow. Examiner withdraws previous rejections and applying new rejections with new references found.

All rejections and objections not explicitly repeated below are withdrawn.

Claim Objections

As per claim 1, the IDE/ATA should not be abbreviated for the initial recital in the claims.

As per claim 2, the SCSI should not be abbreviated for the initial recital in the claims.

As per claim 29, the HDD should not be abbreviated for the initial recital in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,4-11,31,33-38,40-44 rejected under 35 U.S.C. 102 (e) as being anticipated by Jones et al (US 6832281).

As for claim 1, Jones describes a flash-memory card-reader system (Fig 6, Fig 9: multi slots flash memory card reader) comprising: a hard disk controller interface (Fig 9: #46 IDE interface); a buffer coupled to the hard disk controller interface (Jones's Fig 9, column 10 lines 17-21 data is buffered then sent to host's hard drive, re-moveable mass storage); a processing unit coupled to the buffer (Fig 10: #92 CPU column 10 lines 57-65); and a flash-memory card-controller unit coupled to the buffer and to the processing unit (Fig 9: #62; column 8 line 62 to column 9 line 30, teaches circuits to convert); wherein the hard disk controller interface is operable to communicate with a hard disk controller in a host system (Jones's page 2, paragraph

18) , wherein the hard disk controller interface is operable to receive incoming commands from the hard disk controller (Jones's page 2, paragraph 18); and wherein the processing unit is operable to translate the incoming commands to produce translated incoming commands usable by the flash-memory card-controller unit, wherein the processing unit is operable to provide the translated incoming commands to the flash-memory card-controller unit (Jones's Fig 10, pages 3,4 paragraphs 29,30 teach the convert chip's processor operating to convert incoming commands to memory devices using the devices interface's circuits in Fig 9: #62).

As for claim 4, Jones describes wherein the flash-memory card-controller unit is operable to access a flash memory card in response to the translated incoming commands (Jones's Fig 9, column 9 lines 1-10 translated incoming command to access data in compact flash card #16).

As in claim 5, Jones describes a housing comprising at least one slot for receiving memory card (Jones' Fig 6: multi slots memory card reader); wherein the flash-memory card-controller unit is coupled to the housing (Jones's column 9 lines 10-15); wherein the flash-memory card-controller unit is operable to access the flash-memory card in response to the translated incoming commands (Jones's Fig 9, column 9 lines 1-10 translated incoming command to access data in compact flash card #16).

As in claim 6, the claim recites wherein the hard disk controller interface, the buffer; the processing unit, and the flash-memory card-controller unit are comprised in the housing. The claim is rejected based on the same rationale as of claims 1,5.

As in claim 7, Jones teaches wherein the flash-memory card comprises one of a Compact Flash Card, a Secure Digital Card, a Multi Media Card, a Smart Media Card, and a Memory Stick Card (Jones's Fig 7, column 9 lines 15-22).

As in claim 8, the claim is rejected based on the same rationale as of claims 1,5. Jones further describes multiple memory cards are inserted and configured by the converter chip to be operated dynamically (Jones's column 9 lines 22-31).

As in claim 9, the claim is rejected based on the same rationale as of claims 8.

As in claim 10, Jones describes wherein the flash-memory card-reader system appears as a HDD to the host system (Jones's Fig 9 shows the multi memory card reader capable of interface with the host and the external hard drive, Fig 9: #76, thus it appears to the host as a HHD).

As in claim 11, the claim recites wherein the processing unit is operable to: translate outgoing commands issued by the flash-memory card-controller unit to produce translated outgoing commands; and provide the translated outgoing commands to the hard disk controller interface; and wherein the hard disk controller interface is operable to receive the translated outgoing commands and provide the translated outgoing commands to the hard disk controller in the host system. The claim rejected based on the same rationale as of claims 1 and 10.

Claims 31 rejected based on the same rationale as of claim 1.

Claims 33-35 rejected based on the same rationale as in claim 1. Jones further teaches the multi memory card reader are designed and embedded into various portable devices such as PDA, digital camera (see Jones' column 1).

Claim 36 rejected based on the same rationale as of claim 8.

Claim 37 rejected based on the same rationale as of claim 9.

Claim 38 rejected based on the same rationale as of claim 1.

Claim 40 rejected based on the same rationale as of claim 35.

Claim 41 rejected based on the same rationale as in claim 1. Jones clearly teaches the multi memory card devices capable of generating an outgoing command in response to a translated incoming command from a different interface.

Claim 42 rejected based on the same rationale as in the rejection of claim 1. Jones further teaches the interface controller is capable of transferring data and command from flash memory card to host in conjunction and accordingly to IDE protocol.

Claim 43 rejected based on the same rationale as of claim 42.

As in claim 44, various memory media are described in Jones's column 5 lines 35-55.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,16-25,32 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) as applied to claim 1, and in view of Piau et al (US 2004/0049627).

As for claim 2, the claim recites wherein the hard disk controller comprises and IDE/ATA controller; and wherein the incoming commands are ATA commands. Jones's Fig 9, column 9 lines 10-15 teaches a memory card reader system capable of converting commands from host into translated commands being used to transfer data from/to memory device' interface. Jones clearly teaches that the commands for incoming data can be IDE interface, or any other interface such as IEEE 1394. Although Jones does not explicitly state the ATA interface, however, Piau describes a memory controller device having circuits for interfaces such as IDE, and ATA/ PCMIA interfaces (see Piau's Fig 2: #203 ATA). It would have been obvious to one of ordinary skill in the art at the time of invention to include the interfaces circuits as suggested by Piau into Jones to add another interface such as ATA/PCMIA into the memory card reader and thereby further allowing it to communicate with external devices that use widely popular interface such as ATA/PCMIA (Piau's paragraph 18).

Claim 16 rejected based on the same rationale as of claims 1 and 2.

Claims 17,32 rejected based on the same rationale as of claim 2.

Claim 18 rejected based on the same rationale as of claim 4.

Claim 19 rejected based on the same rationale as of claim 5.

Claim 20 rejected based on the same rationale as of claim 6.

Claim 21 rejected based on the same rationale as of claim 7.

Claims 22 rejected based on the same rationale as of claim 8.

Claims 23 rejected based on the same rationale as of claim 9.

Claim 24 rejected based on the same rationale as of claim 10.

Claim 25 rejected based on the same rationale as of claim 11.

Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) as applied to claim 1, and in view of Day et al (US 2004/0019734).

Wherein the hard disk controller comprises a SCSI controller; and wherein the incoming command is SCSI commands. Jones clearly teaches that the commands for incoming data can be IDE interface, or any other interface such as IEEE 1394. Although Jones does not explicitly state the SCSI interface, however, Day describes a memory controller device having circuits for interfaces such as SCSI interface (see Day's Fig 2, paragraph 4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the interfaces circuits as suggested by Day into Jones to add another interface such as SCSI into the memory card reader and thereby further allowing it to communicate with external devices that use another popular interface such as SCSI (Day's paragraph 2).

Claims 12-13,39 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) as applied to claim 11, 38 respectively and in view of Learmonth (US 6941397).

As in claim 12, the claim recites wherein the translated outgoing command comprises ATA commands (claim 12); wherein the translated outgoing command comprises SCSI commands (claim 13). Although Jones does not explicitly state that the translated outgoing command comprises ATA commands and SCSI commands, however, Learmonth discloses a card reader device capable of sending translated outgoing commands comprises ATA commands and SCSI commands (Learmonth's Fig 1#30 card reader system capable of translated outgoing commands into ATA commands and SCSI commands that are used in external devices such has

hard disk, and/or optical storages such as DVD that use ATA and SCSI command interfaces; (see Learmonth's column 3, lines 55-67, column 6 lines 20-34, card reader transfer outgoing command data to optical storages using ATA and SCSI command interfaces). It would have been obvious to one of ordinary skill in the art at the time of invention to include circuits to translate SCSI commands as suggested by Learmonth into Jones's system thereby further allowing it to communicate with external devices that use another popular interface such as SCSI (Learmonth's column 3 lines 55-65).

Claim 39 rejected based on the same rationale as of claim 12.

Claims 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) as applied to claim 1, and in view of Learmonth (US 6941397), Chen et al (2003/0226898).

As in claims 14-15, the claims rejected based on the same rationale as of claims 12-13. The claim further recites an ATA register emulation unit coupled between the buffer and the processing unit, wherein the ATA register emulation unit is configured to store ATA command and status information (claim 14); a SCSI register emulation unit coupled between the buffer and the processing unit, wherein the SCSI register emulation unit is configured to store SCSI command and status information. Although Jones, Learmonth do not explicitly teach the associated registers to configure an interfaces such as ATA and SCSI. However, in order for the card reader to track data and command being transferred in an automatic and concurrently manner, the implementation of these registers are required, Chen discloses a multi memory card reader device having registers to configuring multiple functioning interfaces (Fig 5,

configuration registers, data, status, command registers in order to track control, address, data status state information over interfaces to devices Fig 5: #13, #14). It would have been obvious to one of ordinary skill in the art at the time of invention to include the interfaces control circuits and registers as suggested by Chen into Jones's system thereby allowing multiple concurrently data transfers being tracked in an automatically manner (Chen's paragraph 17).

Claim 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281), Piau et al (US 2004/0049627) as applied to claim 25,and in view of Learmonth (US 6941397).

Claim 26 rejected based on the same rationale as of claim 12.

Claim 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281), Piau et al (US 2004/0049627) as applied to claim 16,and in view of Learmonth (US 6941397), Chen et al (2003/0226898).

Claim 27 rejected based on the same rationale as of claim 14.

Claims 28-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) and in view of Chen et al (2004/0255064).

Claim 28 rejected based on the same rationale as of claim 1. Jones does not explicitly describe the integrated aspect of the multi memory card reader device. However, Chen'064 teaches a multi memory card reader device that can be implemented in an application-integrated chip (see Chen'064's Fig 2: #21). It would have been obvious to one of ordinary skill in the art at

the time of invention to include the application integrated chip as suggested by Chen into Jones's system thereby allowing a single chip that is capable of translating command and transferring data over multiple interfaces in various portable applicant devices such as palm DVD (Chen'064's paragraph 6).

Claim 29 rejected based on the same rationale as of claim 10.

Claim 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al (US 6832281) , Chen et al (2004/0255064) as applied to claim 28, and in view of Learmonth (US 6941397).

Claim 30 rejected based on the same rationale as of claim 12.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yano et al (2004/0041865).

Blood et al (2003/0113351).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 7/21/06

DD

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TC2188

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SUPERVISORY PATENT EXAMINER